REMARKS

Claims 1 - 3 have been canceled by a prior amendment without prejudice or disclaimer of the subject matter thereof. Applicants reserve the right to pursue the subject matter of any of the canceled claims in the subject application and/or subsequently filed continuing applications.

Claims 4 - 7, 20 - 22, and 37 have been amended.

Claims 52 - 57 have been added.

Claims 4 - 57 are present in the subject application.

In the Office Action of August 18, 2009, the Examiner has indicated that claims 19 - 33 are allowed with claims 4 - 33 being allowable over the art of record, has rejected claims 4 - 18 under 35 U.S.C. §101, and has rejected claims 34 - 51 under 35 U.S.C. §112, first paragraph. Favorable reconsideration of the subject application is respectfully requested in view of the following remarks.

Initially, Applicants gratefully acknowledge the courtesies extended by Examiner Jones during a recent telephone Interview to further clarify the outstanding rejections. During the Interview, the Examiner indicated with respect to the rejection under 35 U.S.C. §101 that incorporating hardware into independent claim 4, such as a processor, should overcome the rejection. In addition, the Examiner requested a showing of support for claims 4 - 18 and an indication that the support similarly applies to corresponding ones of claims 34 - 51. The Examiner further indicated that these requested actions should place the application in condition for allowance.

The Examiner has rejected claims 4 - 18 under 35 U.S.C. §101 as being directed toward non-statutory subject matter. The Examiner takes the position that it is not clear from the claims that the computer system requires hardware.

This rejection is respectfully traversed since the term "computer" (recited within independent claim 4) typically refers to hardware. However, in order to expedite prosecution of the subject application, independent claim 4 has been amended to recite the feature of the computer system including at least one processor in accordance with the Examiner's suggestion, while claims 5 - 7, 20 - 22, and 37 have been amended for further clarification. Accordingly, claims 4 - 18 are considered to be directed toward statutory subject matter and comply with 35 U.S.C. §101.

The Examiner has rejected claims 34 - 51 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Examiner takes the position that the claims contain subject matter not described in the specification.

This rejection is respectfully traversed since the claims are fully supported by the specification as discussed below. Initially, Applicants have previously provided an adequate showing of support for independent claim 4 as acknowledged by the Examiner in the Office Action (at Page 3). Independent claims 19 and 34 recite features similar to those of independent claim 4, but are in the form of Program Product Apparatus and Method claims, respectively. Accordingly, the showing of support for independent claim 4 similarly applies to independent claims 19 and 34 and, therefore, these independent claims are considered to be fully supported by the specification and comply with 35 U.S.C. §112, first paragraph.

In accordance with the Examiner's request, the following are example showings of support for dependent claims 5 - 18.

5. The system of claim 4, wherein said virtual machine unit includes:

an instantiation unit to create and delete said nodes in response to instructions received from at least one of said instantiation engine and said evolution engine **(e.g., See Fig. 2, IU; Substitute Specification Pages 8 (Second Paragraph), 11 (Fourth Paragraph), and 24 ("Instantiation Unit (IU)"))**;

a population unit to store and evaluate said data within said nodes in response to instructions received from at least one of said population engine and said evolution engine **(e.g., See Fig. 2, PU; Substitute Specification Pages 8 (Second Paragraph), 11 (Sixth Paragraph), and 24 ("Population Unit (PU)"))**;

a navigation unit to traverse said topology and retrieve information from said selected nodes in response to instructions received from at least one of said navigation engine and said evolution engine **(e.g., See Fig. 2, NU; Substitute Specification Pages 8 (Second Paragraph), 12 (First Paragraph), 14 (Second Paragraph), and 25 ("Navigation Unit (NU)"))**; and

a configuration unit to store parameters defining said topology of said nodes representing said problem and configuration parameters for said hardware architecture in response to instructions received from said configuration engine **(e.g., See Fig. 2, SCU; Substitute Specification Pages 8 (Second Paragraph), 9 (Fourth Paragraph), and 24 ("Solution-Space Configuration Unit (SCU)"))**.

6. The system of claim 5, wherein said computer system further includes:

a virtual assembler to convert said instructions from at least one of said instantiation, population, navigation and evolution engines into a format compatible with said hardware architecture emulated by said virtual machine unit **(e.g., See Fig. 1, NVCL Assembler; Substitute Specification Page 8 (Last Paragraph))**.

7. The system of claim 4, wherein said computer system further includes:

a platform driver unit to interface said virtual machine unit with said computer system, wherein said platform driver unit converts commands for said emulated hardware architecture into commands compatible with said computer system **(e.g., See Fig. 1, Platform Drivers; Substitute Specification Page 9 (First Paragraph))**.

8. The system of claim 4, wherein said virtual operating system includes:

a thread unit to create one or more additional instances of said processing system that each include subsets of said emulated hardware architecture, wherein each instance is associated with a corresponding task to enable said tasks to be performed concurrently **(e.g., See Substitute Specification Pages 9 (Second Paragraph) and 29 (Second Paragraph))**.

9. The system of claim 4, wherein said computer system includes an arithmetic logic unit, and said virtual machine unit further includes:

a virtual arithmetic unit to emulate an arithmetic logic unit of said hardware architecture, and to selectively pass arithmetic operations for said emulated hardware architecture to said arithmetic logic unit of said computer system **(e.g., See Fig. 2, ALU; Substitute Specification Pages 12 (Third Paragraph) and 27 ("Arithmetic & Logic Unit (ALU)"))**.

10. The system of claim 4, wherein said computer system includes at least one of local and distributed networks of processing systems, and said emulated hardware architecture includes a corresponding instruction set **(e.g., See Substitute Specification Pages 5 (First Paragraph), 23 ("VM Unit Descriptions"), and 45 (Table 1))**.

11. The system of claim 4, wherein each node includes an index word and a data word **(e.g., See Substitute Specification Page 21 ("Node"))**.

12. The system of claim 4, wherein each node includes one or more of numeric tags, character tags, boolean flags, numeric values, character values, object identifications, database-record identifications, simple arrays, variable-density multidimensional arrays, symbolic functions, mathematical functions, connection pointers to other nodes, function pointers, look-up-table list pointers, linked-lists, and pointers to other solution spaces, data representations, procedures, or other emulated hardware architectures **(e.g., See Substitute Specification Page 8 (Top Partial Paragraph))**.

13. The system of claim 4, wherein said topology includes at least one of independent point-clouds, ordered sets of points, acyclic graphs, cyclic graphs, balanced trees, recombining graphs, meshes, and lattices **(e.g., See Substitute Specification Page 7 (Second Paragraph))**.

14. The system of claim 9, wherein said virtual arithmetic unit provides fixed-point integer arithmetic with precision indicated by said user software application **(e.g., See Substitute Specification Pages 18 ("optimized calculation") and 27 ("Arithmetic & Logic Unit (ALU)"))**.

15. The system of claim 10, wherein said virtual machine unit includes:

a network unit to manage distribution of data and processes to said networked processing systems **(e.g., See Substitute Specification Page 12 (Fifth Paragraph))**.

16. The system of claim 4, wherein said virtual operating system includes:

a process unit to manage daemons for background processing of said nodes **(e.g., See Substitute Specification Page 7 (First Paragraph))**; and

a toolbox unit to enable performance of frequently-used tasks **(e.g., See Substitute Specification Page 7 (First Paragraph))**.

17. The system of claim 4, wherein said hardware architecture includes a non-Von Neumann architecture **(e.g., See Substitute Specification Page 29 (First Paragraph))**.

18. The system of claim 4, wherein said hardware architecture includes a reduced instruction set computer (RISC) architecture **(e.g., See Substitute Specification Page 19 ("Design Overview"))**.

Dependent claims 20 - 33 and 35 - 48 recite features similar to those of dependent claims 5 - 18, but are in the form of Program Product Apparatus and Method claims, respectively. Accordingly, the showing of support for dependent claims 5 - 18 similarly applies to dependent claims 20 - 33 and 35 - 48 and, therefore, dependent claims 5 - 18, 20 - 33, and 35 - 48 are considered to be fully supported by the specification and comply with 35 U.S.C. §112, first paragraph.

Claims 49 - 51 include some further limitations. The following are example showings of support for these limitations.

49. The method of claim 34, wherein said emulation of said hardware architecture includes employing at least one of a small instruction set, simple and efficient data representation and handling, inherent vector representation, limited data/calculation modes, interleaved memory, table lookup, induced pointers, and distributed and parallelized computation **(e.g., See Substitute Specification Page 18 ("supercomputer techniques"))**.

50. The method of claim 34, wherein step (b.2) further includes:

(b.2.1) pre-computing said data within said nodes of said solution space to enable navigation of possible solutions to occur in near real-time **(e.g., See Substitute Specification Pages 19 ("pre-compute & navigate") and 91 ("2."))**.

51. The method of claim 46, wherein said daemons operate concurrently to perform tasks including at least one of collecting garbage, pruning trees, condensing redundancies, processing edit-queues, interpolating with finer granularity around selected nodes in said solution space, and extrapolating and elaborating said data during processing and navigation of said nodes **(e.g., See Substitute Specification Page 7 (First Paragraph) and 19 ("autonomous daemons"))**.

Accordingly, claims 49 - 51 are considered to be fully supported by the specification and comply with 35 U.S.C. §112, first paragraph.

New claims 52 - 54 and 55 - 57 recite features similar to those of dependent claims 49 - 51, but depend from System and Program Product Apparatus claims, respectively. Accordingly, the showing of support for dependent claims 49 - 51 similarly applies to new claims 52 - 57 and, therefore, dependent claims 52 - 57 are considered to be fully supported by the specification and comply with 35 U.S.C. §112, first paragraph.

In view of the foregoing, Applicants respectfully request the Examiner to find the application to be in condition for allowance with claims 4 - 57. However, if for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is

respectfully requested to call the undersigned attorney to discuss any unresolved issues and to expedite the disposition of the application.

Applicants hereby petition for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

Dated: 02/12/10

Respectfully submitted by:

/Stuart B. Shapiro/

Stuart B. Shapiro
Reg. No. 40169

EDELL, SHAPIRO & FINNAN, LLC
CUSTOMER NO.
1901 Research Boulevard, Suite 400
Rockville, MD 20850
(301) 424-3640